PTO/SB/05 (Modified)

jc685 U.S. PTO 10/20/00

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	95-384
First Named Inventor or Application Identifier:	FAROOQ

Title: ARRANGEMENT FOR CONVERTING BETWEEN A MEDIA INDEPENDENT INTERFACE AND A TWISTED PAIR MEDIUM USING A FIELD PROGRAMMABLE GATE ARRAY

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO:
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Washington, DC 20231

jc542 U.S. PTO 09/691913 10/20/00

1. [X] Fee Transmittal Form
2. [X] Specification, Claims & Abstract ..... [Total Pages: 9]
3. [X] Formal Drawing(s) *(35 USC 113)* .... [Total Sheets: 2]
4. [X] Oath or Declaration ..... [Total Pages: 2]
   a. [X] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional with Box 17 completed)*
      i. [ ] DELETION OF INVENTOR(S)
      Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. [ ] Incorporation by Reference (usable if Box 4b is checked)
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. [ ] Microfiche Computer Program *(Appendix)*
7. [ ] Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [X] Assignment Papers (cover sheet & document(s))
9. [ ] 37 CFR 3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12. [ ] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
14. [ ] Small Entity Statement(s) [ ] Statement filed in prior application, status still proper and desired.
15. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. [ ] Other: Claim of Priority

17. If a CONTINUING APPLICATION, *check appropriate box and supply the requisite information:*

[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No: ___/_____

18. CORRESPONDENCE ADDRESS

Leon R. Turkevich
Farkas & Manelli, PLLC
2000 M Street, N.W., 7th Floor
Washington, D.C. 20036-3307
CUSTOMER NO.: 20736

Name (Type)	Leon R. Turkevich	Registration No. (Att./Agent)	34,035
Signature		Date	October 20, 2000

F & M Form (12/97)

NEW APPLICATION FEE TRANSMITTAL		Attorney Docket No.	95-384
		Application Number	
		Filing Date	October 20, 2000
AMOUNT ENCLOSED	$750.00	First Named Inventor	FAROOQ

FEE CALCULATION (fees effective 12/29/99)

CLAIMS	(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) CALCULATIONS
	TOTAL CLAIMS	10 - 20 =	0	X $ 18.00 =	
	INDEPENDENT CLAIMS	2 - 3 =	0	X $ 80.00 =	
	MULTIPLE DEPENDENT CLAIMS (any number; if applicable)			+ $270.00 =	
			BASIC FILING FEE		+710.00
			Total of above Calculations =		$ 710.00
	Surcharge for late filing fee, Statement or Power of Attorney ($130.00)				+
	Reduction by 50% for filing by small entity (37 CFR 1.9, 1.27 & 1.28).				
			TOTAL FILING FEE =		$710.00
	Surcharge for filing non-English language application ($130.00; 37 CFR 1.52(d))				+
	Recordation of Assignment ($40.00; 37 CFR 1.21(h)(1))				+ 40.00
			TOTAL FEES DUE =		$750.00

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Deposit Account Name	FARKAS & MANELLI	

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SUBMITTED BY: FARKAS & MANELLI, PLLC

Typed Name	Leon R. Turkevich	Reg. No.	34,035
Signature		Date	October 20, 2000

F0742 / 95-384

ARRANGEMENT FOR CONVERTING BETWEEN A MEDIA INDEPENDENT INTERFACE AND A TWISTED PAIR MEDIUM USING A FIELD PROGRAMMABLE GATE ARRAY

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

The present invention relates to testing of integrated network devices such as integrated network switches configured for switching data packets between subnetworks, and the conversion of network data between a media independent interface and a prescribed medium such as 10 Base-T twisted pair.

BACKGROUND ART

Local area networks use a network cable or other media to link stations on the network. Each local area network architecture uses a media access control (MAC) enabling network interface devices at each network node to access the network medium.

Switched local area networks such as Ethernet (IEEE 802.3) based systems are encountering increasing demands for higher speed connectivity, more flexible switching performance, and the ability to accommodate more complex network architectures. Hence, network switch designers and test engineers need to be able to minimize the time and expense needed to evaluate designs during prototyping of Ethernet-based network systems.

One problem associated with prototyping network-based switch chips involves the relatively complex interconnections between test system components that affect test system reliability. For example, Figure 1 is a diagram illustrating a conventional test setup 10, including emulation hardware 12 simulating network traffic, a target device under test 14, for example an integrated multiport switch as illustrated in commonly-assigned U.S. Patent No. 5,953,335, test logic 16, and a test instrument 18. The test logic 16, implemented for example as a field programmable gate array, is configured for performing prescribed logic functions based on reception of network signals from the target device under test 14 across a first media independent interface (MII) 20a, and outputting modified network signals to the test instrument 18 across a second media independent interface 20b. For example, the test logic 16 may be configured for buffering between the first MII 20a operating at 250kbps, and the second MII operating at 10Mbps. Hence, the test logic 16 provides compatability between the target

device 14, operating under sub-network speeds during testing, and the test instrument 18 configured for operating at prescribed network data rates.

Use of the media independent interfaces 20 for transfer of data requires use of MII cables, resulting in a relatively complex test configuration that affect test efficiency and reliability. Unfortunately, commercially available physical layer transceivers operate under a fixed clock speed; hence, the relative inflexibility of commercially available physical layer transceivers render then unsuitable for use in the above-described test system 10 in an effort to reduce test system complexity by replacing the media independent interface 20b with a less complex interface.

SUMMARY OF THE INVENTION

There is a need for an arrangement that enables a prototype network system to be developed and tested without the necessity of complex network-based interfaces, such as media independent interfaces.

There also is a need for an arrangement that enables a prototype network system to be developed using conventional twisted pair media, without the necessity of physical layer transceivers having fixed clock speeds.

These and other needs are attained by the present invention, where an integrated network test device has network logic configured for performing prescribed network device operations and outputting network data based on a media independent interface (MII) based protocol, first test logic configured for performing prescribed test operations on the network data and outputting test data based on the MII-based protocol, and second test logic configured for converting the test data, output from the first test logic according to the MII-based protocol, into analog-based signals for transmission on twisted pair media. The integration of the network logic, the first test logic, and the second test logic dramatically simplifies testing systems, since the integrated network test device can be coupled to test equipment such as a traffic generator, using a relatively simple twisted pair or 10 BaseT connection, as opposed to more complex MII cabling.

One aspect of the present invention provides a method in an integrated test device. The method includes performing, using network logic on the integrated test device, first network device operations on received data and outputting network data according to a media independent interface (MII) based protocol. The method also includes performing prescribed test operations on the network data using first test logic on the integrated test device and outputting test data based on the MII-based protocol. The method also includes converting the test data into analog-based signals for transmission on a prescribed network medium using second test logic on the integrated test device.

Another aspect of the present invention provides an integrated network test device. The integrated network test device includes network logic configured for performing prescribed network device operations and outputting network data based on a media independent interface (MII) based protocol. The integrated network test device also includes first test logic configured for performing prescribed test operations on the network data and outputting test data based on the MII-based protocol, and second test logic configured for converting the test data, output from the first test logic according to the MII-based protocol, into analog-based signals for transmission on a prescribed network medium.

Additional advantages and novel features of the invention will be set forth in part in the description which follows and in part will become apparent to those skilled in the art upon examination of the following or may be learned by practice of the invention. The advantages of the present invention may be realized and attained by means of instrumentalities and combinations particularly pointed in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

Reference is made to the attached drawings, wherein elements having the same reference numeral designations represent like elements throughout and wherein:

Figure 1 is a block diagram of a conventional system configured for testing a prototype network design using a target device under test.

Figure 2 is a diagram illustrating a system for testing a prototype network using an integrated network test device according to an embodiment of the present invention.

Figure 3 is a diagram illustrating in detail the interface conversion logic of Figure 2.

BEST MODE FOR CARRYING OUT THE INVENTION

Figure 2 is a block diagram illustrating a testing system 30 configured for testing an integrated (i.e., single chip) network test device 32. The integrated network test device 32 is configured for receiving data, such as simulated network data, from the emulation hardware 12 across multiple data paths 34. For example, each link 34 may represent an MII-based link for transfer of network data from a simulated link partner.

The integrated network test device 32 includes network logic 36, first test logic 38 implemented using a field programmable gate array, and second test logic 40 implemented using a field programmable gate array. The network logic 36 is configured for performing prescribed network device operations, for example performing switching operations to simulate the network switch 14 as described in the above-

identified U.S. Patent No. 5,953,335. In particular, the network logic 36 includes all or at least part of the components of the simulated network switch necessary to test the logic and operational performance of the network switch prior to commercial production.

At least one network switch port of the network logic 36 is configured for sending and receiving network data across a low speed MII interface 42, for example according to a 250 kilohertz clock. The first test logic 38 is configured for performing prescribed test operations that may be programmed into the field programmable gate array, for example checking valid checksum, etc.. Alternatively, the first test logic 38 may merely be configured for converting the network data received according to the 250 kilohertz clock into an IEEE 802.3 compliant data stream, for example into test data output onto a media independent interface 44 using a 10 MHz clock, resulting in a data rate of 10 Mbps or 100 Mbps, as needed.

As described above, commercially available physical layer transceivers have a fixed clock speed, hence they cannot accommodate variations in the data rate on the MII 44 which may be necessary during testing or evaluation of the network logic 36.

According to the disclosed embodiment, use of an integrated network test device 32 enables features to be selectively added or subtracted from the integrated network test device as necessary for optimum testing conditions. In particular, the integrated network test device 32 includes second test logic 40, implemented using a field programmable gate array, for converting the test data output onto the MII interface 44 from the first test logic 38 into analog-based signals for transmission on twisted pair media 46 to the test instrument 18'. Hence, the system 30 can be established without the necessity of MII cables between the target device under test (illustrated as the network logic 36) and the test instrument 18', for example the traffic generator.

Figure 3 is a block diagram illustrating the second test logic 40, also referred to as an MII to twisted pair converter, according to an embodiment of the present invention. In particular, the second test logic 40 implements into a field programmable gate array the logic from the commercially-available Am79C873 NetPHY™-1 10/100 Mbps Ethernet Physical Layer Single-Chip Transceiver with 100BASE-FX Support from Advanced Micro Devices, Inc., Sunnyvale California.

The MII to twisted pair converter 40 includes a 10Base-T transceiver portion 50, a 100 Base transmitter portion 52, a 100 Base receiver portion 54, and MII interface control portion 54, and modules for collision detection 56, carrier sense 58, and autonegotiation 60.

The 100 base transmitter portion 52 includes an encoder 62 configured for converting 4-bit (4B) nibble data generated by the MAC reconciliation layer into a 5-bit (5B) coded group for transmission. The scrambler 64 scrambles the data stream with sufficient randomization to decrease radiated emissions by spreading the transmit energy across the frequency spectrum. The parallel to serial converter 66 serializes

the 5-bit scrambled data into a serial data stream, and the converter 68 performs Non-Return to Zero Interface (NRZI) encoding for compatibility with the TP-PMD standard for 100 Base-TX transmission over Category-5 unshielded twisted pair cable, such as the twisted pair cable 46. If desired, a pseudo ECL (PECL) driver 70 is configured for converting the NRZI coded data into PECL single levels for transmission over fiber media.

The 100 Base transmitter portion 52 also includes an MLT-3 (multiple layer transition) converter 72 for converting the NRZI and coded data stream into two binary data streams with alternately phased logic one events. The two binary data streams are output to the twisted pair output driver 74 which converts the data streams to analog current sources based on a rise/fall-time controller 76.

The 100 Base receiver 54 includes an adaptive equalizer 80 configured for compensating for attenuation in received analog data signals from a copper twisted pair cable 46. The compensated analog data signals in MLT-3 format are decoded into NRZI signals by the decoder 82, which outputs the NRZI signals to the clock recovery module 84. The receiver 54 also includes a PECL receiver 86 configured for receiving PECL signal level data from an optical medium, and outputting the received signals to the clock recovery module 84. Note that the clock recovery module 84 maybe controlled by digital logic 87.

The decoder 88 recovers the NRZ data stream from the NRZI signals output by the decoder 82, and the serial NRZ data stream is converted into 5-bit data by the serial to parallel converter 90. The descrambler 92 descrambles the received data stream, and the code group alignment module 94 converts the unaligned 5-bit data into 5-bit code group data. The decoder 62 than converts the 5-bit code groups into 4-bit nibble data for transfer by the MII interface controller to the MII 44.

Additional details regarding the operation of the MII to the twisted pair converter 40 of Figure 3 are described in the data sheet (Preliminary) for the above-identified Am79C873 transceiver from Advanced Micro Devices (Publication No. 22164, Issued February, 1999).

According to the disclosed embodiment, an integrated network test device enables network logic to be tested using prescribed network media for interconnection with test instruments, without the necessity of commercially available physical layer transceivers that may have insufficient flexibility to accommodate variations during testing of the network logic. Hence, testing systems maybe developed without the necessity of MII cables between a target device under test and the test equipment, reducing the complexity of the test system. In addition, modules can selectively be added or deleted from the field programmable gate array in the converter 40; hence, a simple twister pair converter may be implemented merely by maintaining the 10Base-T module 50 within the logic 40.

While this invention has been described with what is presently considered to be the most practical preferred embodiment, it is to be understood that the invention is not limited to the disclosed

embodiments, but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims.

What is Claimed Is:

1. A method in an integrated test device, the method comprising:

performing, using network logic on the integrated test device, first network device operations on received data and outputting network data according to a media independent interface (MII) based protocol;

performing prescribed test operations on the network data using first test logic on the integrated test device and outputting test data based on the MII-based protocol; and

converting the test data into analog-based signals for transmission on a prescribed network medium using second test logic on the integrated test device.

2. The method of claim 1, wherein the step of performing first network device operations includes switching the received data according to prescribed switching logic.

3. The method of claim 2, wherein the step of performing prescribed test operations includes second converting the network data, having a first data rate, into the test data having a second data rate substantially greater than the first data rate.

4. The method of claim 3, wherein the first data rate is about 250 kbps and the second data rate is about 10Mbps.

5. The method of claim 1, wherein the converting step includes converting the test data into 10 Base-T compliant analog signals.

6. The method of claim 1, wherein the converting step includes converting the test data into 100 Base compliant analog signals.

7. An integrated network test device comprising:

network logic configured for performing prescribed network device operations and outputting network data based on a media independent interface (MII) based protocol;

first test logic configured for performing prescribed test operations on the network data and outputting test data based on the MII-based protocol; and

second test logic configured for converting the test data, output from the first test logic according to the MII-based protocol, into analog-based signals for transmission on a prescribed network medium.

8. The device of claim 7, wherein the second test logic is configured for converting the test data into 10 Base-T compliant analog-based signals.

9. The device of claim 7, wherein the second test logic is configured for converting the test data into 100 Base compliant analog-based signals.

10. The device of claim 7, wherein , wherein the first test logic is configured for converting the network data, having a first data rate of about 250 kbps, to the test data having a second data rate of about 10Mbps.

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ARRANGEMENT FOR CONVERTING BETWEEN A MEDIA INDEPENDENT INTERFACE AND A TWISTED PAIR MEDIUM USING A FIELD PROGRAMMABLE GATE ARRAY

ABSTRACT OF THE DISCLOSURE

An integrated network test device has network logic configured for performing prescribed network device operations and outputting network data based on a media independent interface (MII) based protocol, first test logic configured for performing prescribed test operations on the network data and outputting test data based on the MII-based protocol, and second test logic configured for converting the test data, output from the first test logic according to the MII-based protocol, into analog-based signals for transmission on twisted pair media. The integration of the network logic, the first test logic, and the second test logic dramatically simplifies testing systems, since the integrated network test device can be coupled to test equipment such as a traffic generator, using a relatively simple twisted pair or 10 BaseT connection, as opposed to more complex MII cabling.

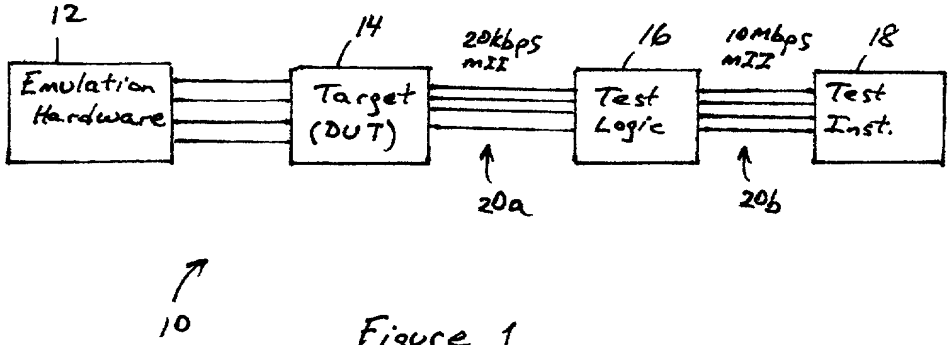

Figure 1
(Prior Art)

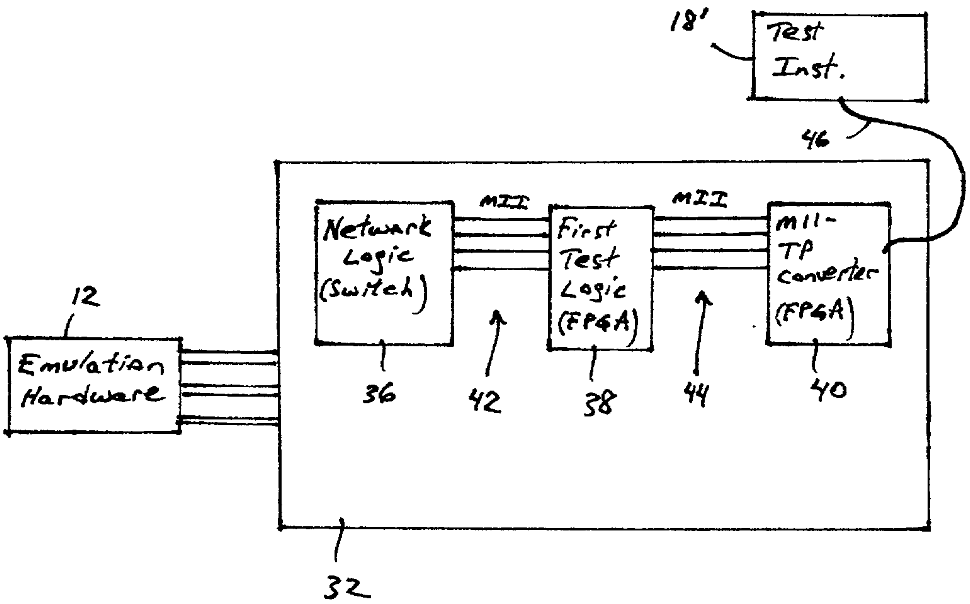

Figure 2

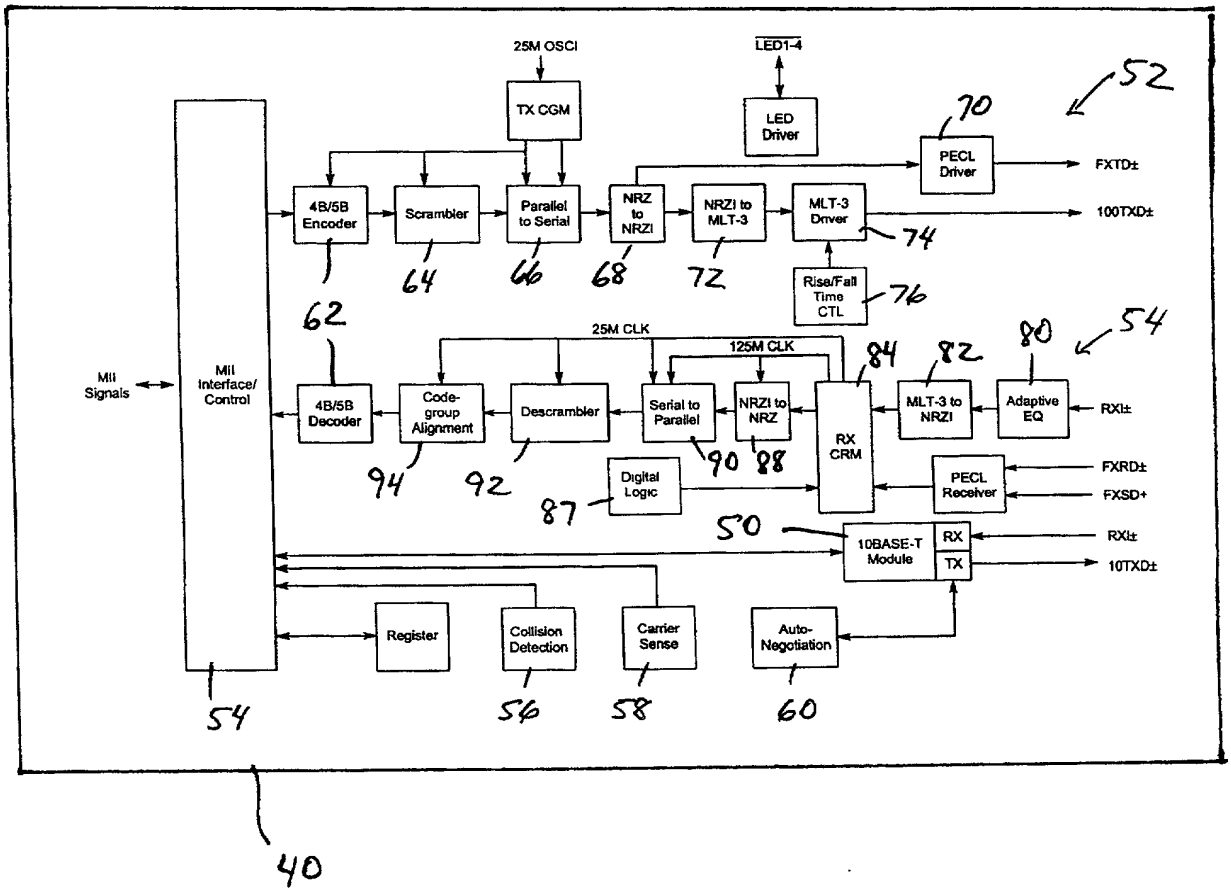
25M OSCI
TX CGM
LED1-4
LED Driver
52
70
PECL Driver
FXTD±
100TXD±
4B/5B Encoder
Scrambler
Parallel to Serial
NRZ to NRZI
NRZI to MLT-3
MLT-3 Driver
74
64
66
68
72
Rise/Fall Time CTL
76
62
25M CLK
125M CLK
84
82
80
54
MII Signals
MII Interface/ Control
4B/5B Decoder
Code-group Alignment
Descrambler
Serial to Parallel
NRZI to NRZ
RX CRM
MLT-3 to NRZI
Adaptive EQ
RXI±
94
92
90
88
Digital Logic
87
PECL Receiver
FXRD±
FXSD+
50
10BASE-T Module
RX
TX
RXI±
10TXD±
Register
Collision Detection
Carrier Sense
Auto-Negotiation
54
56
58
60
40

Figure 3

Docket No. 95-384

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter claimed and for which a patent is sought on the invention entitled **ARRANGEMENT FOR CONVERTING BETWEEN A MEDIA INDEPENDENT INTERFACE AND A TWISTED PAIR MEDIUM USING A FIELD PROGRAMMABLE GATE ARRAY**

[X] is attached hereto [ ] was filed on as Application Serial No. and was amended on (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is known to me to be material to patentability in accordance with Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d) or Section 365(b) of any foreign application(s) for patent or inventor's certificate, or Section 365(a) of any PCT international application which designated at least one country other than the United States, listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):			**Priority Claimed**	
Number	**Country**	**Day/Month/Year filed**	**Yes**	**No**

I hereby claim the benefit under 35 USC §119(e) of any United States provisional application(s) listed below.

Prior Provisional Application(s):

Application Number	**Filing Date**

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or Section 365(c) of any PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Prior U. S. Application(s):

Serial No.	**Filing Date**	**Status: Patented, Pending, Abandoned**

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

I hereby appoint the following attorney(s) and/or agent(s): Leon R. Turkevich, Reg. No. 34,035, and the attorneys of Customer No. 20736, all of:

FARKAS & MANELLI, PLLC
2000 M Street, N.W., 7th Floor
Washington, D.C. 20036-3307

and Richard J. Roddy, Reg. No. 27,688, Paul S. Drake, Reg. No. 33,491, Elizabeth A. Apperley, Reg. No. 36,428, Harry A. Wolin, Reg. No. 32,638, Bradley Botsch, Reg. No. 34,552, and Michael Caywood, Reg. No. 37,797, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith, and all future correspondence should be addressed to Customer No. 20736.

****

Full name of sole or first inventor: Rizwan M. Farooq	
Inventor's signature: *Rizwan Farooq*	Date: 10/17/00
Residence: 2868 Homestead Rd. #10, Santa Clara, CA 95051	
Citizenship: Pakistan	
Post Office Address: same as above	